PATENT APPLICATION TRANSMITTAL LETTER

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Transmitted herewith for filing is the patent application of:

Eran Gureshnik, Daniel Yellin, Shlomo Yakobovich and Arie Stalberg

for PULSE MODULATED DIGITAL TO ANALOG CONVERTER (DAC)

Enclosed are:

(X) 17 pages of specification and claims.
(X) Abstract
(X) 5 sheet(s) of Formal Drawings.
(X) Declaration and Power of Attorney (UNEXECUTED)
( ) Statement to establish small entity status of Small Business Concern under 37 CFR 1.9 and 1.27.
( ) Information Disclosure Statement
( ) Assignment and Assignment Recordation
( ) Preliminary Amendment
( ) A check in the amount of $_______ to cover the filing fee.
( ) Any filing fees or presentation of extra claim fees may be charged to Deposit Account No. _______ (Eitan, Pearl, Latzer & Cohen-Zedek)

CLAIMS AS FILED			SMALL ENTITY			OTHER THAN A SMALL ENTITY	
FOR	# FILED	# EXTRA	RATE	FEE	OR	RATE	FEE
BASIC FEE				$380.00			$760.00
TOTAL CLAIMS	11-20		x$ 9	$		x$ 18=	$
INDEP. CLAIMS	6-3	3	x$ 39	$		x$ 78=	$234.00
MULTIPLE DEP. CLAIM PRESENT			x$130=	$		x$260=	$
				$		TOTAL	$994.00

Respectfully submitted,

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2588us.doc

PULSE MODULATED DIGITAL TO ANALOG CONVERTER (DAC)

Eran GURESHNIK, Daniel YELLIN, Shlomo YAKOBOVICH and Arie STALBERG

FIELD OF THE INVENTION

The present invention relates to digital to analog converters, in general, and to pulse density modulation (PDM) digital to analog converters, in particular.

BACKGROUND OF THE INVENTION

As part of the ever present drive to reduce the cost, size and power consumption of electronic devices, smaller and simpler components are being used in the design of these devices. Some of these components are driven by analog control signals and require a stable, high-resolution analog control signal in order to work efficiently. The analog control signals are typically produced by digital to analog converters (DACs). In portable cellular telephones, for example, analog control signals are used to determine the working point of a transmission Automatic Gain Control (AGC), which controls the power of an amplifier of a transmitting device. Analog control signals are also used to determine the working point of a voltage-controlled temperature-compensated oscillator (VCTCXO), which is used to modulate the transmitted signal and to demodulate the received signal.

Conventional DACs use various circuits that are known in the art, for example, resistor ladders. Analog circuits such as resistor ladders require a large silicon area when implemented into an integrated complementary metal

oxide semiconductor (CMOS) circuit, a factor which becomes much more significant from a cost perspective when small sub-micron CMOS technology is used.

Digital to analog converters (DAC) based on pulse width modulation (PWM) or pulse density modulation (PDM) methods are known in the art. The PDM method is described in US Patent 5,337,338 to Sutton et al. A pulse modulated DAC comprises a digital circuit which converts a multi-bit digital signal to a single bit digital signal, followed by an analog low pass filter (LPF) which converts the single bit digital signal to a constant level analog signal. The LPF filters out the undesired high frequencies in the single bit digital signal. A simple and economical way to implement a low pass filter is by using one resistor and one capacitor.

The purpose of the analog LPF is to produce a stable analog signal output that is the average of the discrete levels of the single bit digital signal input. One of the disadvantages of the PWM and PDM methods is that the analog signal output is not constant, but rather has an inherent harmonic ripple in it due to the charging and discharging of the capacitor. This ripple adversely affects the analog components controlled by the analog signal output. For example, a ripple imposed onto an AGC modulates the carrier frequency and generates undesired spurious transmission signals. A ripple imposed onto a VCTCXO will generate spurious replicas of the desired transmission signal at multiples of the ripple frequency, and will interfere with the desired received signal. Another disadvantage is that when the pulse modulated signal changes to represent a different multi-bit digital signal, a relatively long response time is required until the LPF output reaches the new desired value. These two

disadvantages are related: trying to reduce the ripple by decreasing the cutoff frequency results in a slower response time.

Various digital to analog converters, using PWM or PDM methods, are described in the US Patents 5,774,084 to Brombaugh et al., 5,764,165 to Buch, 5,712,636 to Buch, and 5,784,019 to Wong et al. US Patent 5,617,060 to Wilson et al. describes an automatic gain control (AGC) and DC offset correction method and apparatus that uses PDM and a conventional low pass filter. US Patent 5,204,594 to Carbolante discloses a circuit for providing a signal proportional to the average current flowing through coils of a motor operated in both linear and PWM modes.

SUMMARY OF THE INVENTION

There is provided in accordance with a preferred embodiment of the present invention a switchable low pass filter including a first switch connected to a first resistive element, a second switch connected to a second resistive element, and a capacitive element connected to the first and second resistive elements. The switchable low pass filter also includes a controller connected to the first switch and the second switch, the controller operative to open and close at least one of the first switch and the second switch.

Moreover, in accordance with a preferred embodiment of the present invention, the first resistive element has a resistance which is smaller than the resistance of the second resistive element.

There is also provided in accordance with a preferred embodiment of the present invention a device including a plurality of resistive elements, at least one switch connected to one of the resistive elements, and a capacitive element connected to the resistive elements. The capacitive element forms a low pass filter with the resistive elements. The device also includes a controller connected to the at least one switch, the controller operative to open and close the at least one switch thereby switching the resistance of the low pass filter.

There is also provided in accordance with a preferred embodiment of the present invention a device including a plurality of resistive elements, at least one switch connected to one of the resistive elements, and a capacitive element connected to the resistive elements. The capacitive element forms a low pass filter with the resistive elements, and the low pass filter has a response time. The device also includes a controller connected to the at least

one switch, the controller operative to open and close the at least one switch thereby changing the response time.

There is also provided in accordance with a preferred embodiment of the present invention a digital to analog converter. The digital to analog converter includes a digital circuit which produces a pulse modulated signal, and a switchable low pass filter having a plurality of response times for converting the pulse modulated signal to an analog signal having ripples. Switching the low pass filter among the response times changes the size of the ripples.

Moreover, in accordance with a preferred embodiment of the present invention, the digital circuit is a pulse width modulation circuit or a pulse density modulation circuit.

Furthermore, in accordance with a preferred embodiment of the present invention, the switchable low filter includes a first switch connected to a first resistive element, a second switch connected to a second resistive element, and a capacitive element connected to the first and second resistive elements. The switchable low pass filter also includes a controller connected to the first switch and the second switch, the controller operative to open and close at least one of the first switch and the second switch.

Additionally, in accordance with a preferred embodiment of the present invention, the first resistive element has a resistance which is smaller than the resistance of the second resistive element.

There is also provided in accordance with a preferred embodiment of the present invention a device for producing a pulse density modulated signal whose pulse timing is jittered. The device includes a flip flop for storing a value,

a random number generator for producing a substantially random number, and an adder. The adder adds the substantially random number and a multi-bit number to the value. The adder has an upper limit. A pulse is produced when the sum of the substantially random number, the multi-bit number and the value exceeds the upper limit.

There is also provided in accordance with a preferred embodiment of the present invention a method for producing a pulse density modulated signal whose pulse timing is jittered. The method includes the following steps: adding a substantially random number and a multi-bit number to a value stored in a flip flop, thereby producing a sum; if the sum is less than an upper limit, storing the sum in the flip flop, thereby replacing the value; if the sum is not less than the upper limit, producing a pulse, subtracting the upper limit from the sum, thereby producing a result, and storing the result in a flip flop; and repeating the steps.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the appended drawings in which like reference characters identify correspondingly throughout and wherein:

Fig. 1 is a schematic illustration of a portion of an integrated circuit having a DAC of a preferred embodiment of the present invention implemented in it;

Fig. 2A is an exemplary graphical illustration of a pulse modulated signal as a function of time;

Figs. 2B, 2C and 2D are exemplary graphical illustrations of the output analog signal of Fig. 1 as a function of time;

Fig. 3 is a schematic illustration of the digital converter of Fig. 1, according to a preferred embodiment of the present invention;

Fig. 4 is an exemplary graphical illustration of pulse modulated digital signals as a function of time; and

Fig 5 is a schematic illustration of a modified version of the digital converter of Fig. 3, according to a further preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

The present invention is directed to a digital to analog converter (DAC) and to methods of operating a digital to analog converter. The DAC of the present invention is small in size due to the small number of analog components and has relatively low power consumption.

Reference is now made to Fig. 1, which is a schematic illustration of a portion of an integrated circuit 100, having a DAC of a preferred embodiment of the present invention implemented in it. Reference is made additionally to Fig. 2A, which is an exemplary graphical illustration of a pulse modulated signal as a function of time, and to Figs. 2B, 2C and 2D, which are exemplary graphical illustrations of the output analog signal of Fig. 1 as a function of time. In Figs. 2B, 2C and 2D, the horizontal line 201 indicates the desired constant analog signal.

The DAC comprises a digital converter 102, a switchable low pass filter (LPF) 104, an amplifier 108 and a buffer 110. The digital converter 102 converts a multi-bit digital signal to a single bit digital signal, for example using pulse width modulation (PWM) or pulse density modulation (PDM) methods to create a pulse modulated signal.

The switchable LPF 104 receives the single bit digital signal and produces an analog signal. The switchable LPF 104 comprises a first switch SW1 connected to a first resistor R1, a second switch SW2 connected to a second resistor R2, a capacitor C connected serially to the resistors R1 and R2, and a controller 106. The resistors R1 and R2 are connected in parallel. The resistance of the first resistor R1 is small relative to the resistance of the

second resistor R2. In a non-limiting example, the resistance of the first resistor R1 is ten times smaller than the resistance of the second resistor R2.

The controller 106 is operative to open and close switches SW1 and SW2, thereby creating one of three modes of operation of the low pass filter 104.

a) Fast response – large ripple mode

When the switch SW1 is closed and the switch SW2 is open, the low pass filter formed by the resistor R1 and the capacitor C has a fast response time T_1, and a large ripple in the steady-state. This is shown in Fig. 2B by the solid line graph 200. As is known in the art, the ripple frequency coincides with the pulse frequency.

b) Slow response – small ripple mode

When the switch SW1 is open and the switch SW2 is closed, the low pass filter formed by the resistor R2 and the capacitor C has a slow response time T_2, and a small ripple in the steady-state. This is shown in Fig. 2B by the dotted-line graph 202. As is known in the art, the ripple frequency coincides with the pulse frequency.

c) Hold mode

When both the switches SW1 and SW2 are open, the capacitor C is in hold mode, and its voltage level remains almost steady, decreasing slowly in time due to parasitic leakage and leakage through the resistors and switches. This is shown in Fig. 2B by the flat dashed line 204.

According to a preferred embodiment of the present invention, the DAC achieves a fast response time and a small ripple in the steady-state. When the multi-bit digital signal changes, resulting in a new single bit digital signal, the

controller 106 closes switch SW1 and opens switch SW2 so that the capacitor C will charge in the fast response mode. This is shown in Fig. 2C by the solid-line graph 206. When the capacitor C reaches the desired voltage level at time T_1, the controller 106 opens switch SW1 and closes switch SW2 so that the capacitor C will retain its desired voltage level with a small ripple. This is shown in Fig. 2C by the dotted-line graph 208. In such a way, the DAC takes advantage of the fast response mode while the capacitor C is charging, and takes advantage of the small ripple mode when the capacitor C is close to or already at the desired voltage level. As a result, the DAC of the present invention produces a far more stable analog control signal than that of a conventional pulse modulated DAC.

According to another preferred embodiment of the invention, the DAC achieves a fast response time and no ripple in the steady-state. When the multi-bit digital signal changes, resulting in a new single bit digital signal, the controller 106 closes switch SW1 and opens switch SW2 so that the capacitor C will charge in the fast response mode. This is shown in Fig. 2D by the solid-line graph 210. When the capacitor C reaches the desired voltage level at time T_1, the controller 106 opens switch SW1 and closes switch SW2 so that the capacitor C will retain its desired voltage level with a small ripple. This is shown in Fig. 2D by the dotted-line graph 212. When a no-ripple, very stable analog signal is required at beginning at time T_3, the controller 106 opens both switches SW1 and SW2 so that the capacitor C will retain its voltage level in hold mode. This is shown in Fig. 2D by the almost flat dashed line 214.

The motivation for this preferred embodiment is that there are cases, such as control signals for time division multiple access (TDMA) applications,

where a very stable, slowly decreasing signal is preferable to even a small ripple. In such applications, the controller is set so that the time T_3 precedes or substantially coincides with the time at which the analog control signal is needed.

A further advantage of this preferred embodiment is that during hold mode, the switchable LPF 104 draws no current, and the digital converter 102 can be turned off, resulting in a reduction in the overall power consumption.

It will be appreciated that the controller 106 may close both switches SW1 and SW2 when a particularly small resistance is desired.

The operation of the digital converter 102 of Fig. 1 will now be explained with respect to Figs. 3 and 4, to which reference is now made. Fig. 3 is a schematic illustration of a pulse density modulation (PDM) digital converter, according to a preferred embodiment of the present invention.

The digital converter 102 comprises an adder 302 and a flip-flop 304. Initially, the flip-flop has a value of 0. With each cycle of a clock 306, the adder 302 adds the N-bit digital signal input, which is a number having a value between 0 and 2^{N-1}, to the value stored in the flip-flop 304. When the adder 302 reaches or passes the value 2^{N-1}, a pulse is generated. Any remaining value of the adder 302 beyond 2^{N-1} is sent to the flip-flop 304 to be added in the next clock cycle. In such a way, a signal is generated with pulses whose density is proportional to the N-bit digital signal input. This signal is shown by the solid-line graph in Fig. 4, which is an exemplary graphical illustration of the voltage of the pulse modulated digital signal of Fig. 3 as a function of time.

According to a further preferred embodiment of the present invention, the DAC spreads the spectral properties of the harmonic ripple using random

noise. As is known in the art, a PDM signal is composed of pulses whose density is proportional to the value of the multi-bit digital input signal. The frequency of these pulses, known as the ripple frequency, appears in the output analog signal and interferes with the desired signal. The same problem occurs with the output analog signal of a PWM signal, although its ripple frequency is generally lower than that generated by a PDM signal. In the further preferred embodiment of the present invention, the timing of the pulses in the pulse modulated signal is adjusted by a small, random factor, thereby spreading the spectral properties of the harmonic ripple. Reference is now made additionally to Fig. 5, which is a schematic illustration of a modified version of the digital converter of Fig. 3, according to a further preferred embodiment of the present invention. In addition to the adder 302 and the flip-flop 304, the digital converter 102 comprises a uniform distribution random number generator 500 and an additional adder 502. The random number generator 500, for example a pseudo-random number (PN) generator, which is known in the art, is driven by a clock 504. For each cycle of the clock 504, the random number generator 500 generates a random number in the range –M to +M, where M is significantly smaller than N. The adder 502 adds the random number to the value in the flip flop 304, and the result is added by the adder 302 to the N-bit digital signal input. The resulting pulse modulated signal is shown in Fig. 4 by the dashed-line graph. The effect is that the pulses generated by the digital converter of Fig. 5 are slightly offset in time ("jittered") from the pulses generated by the digital converter of Fig. 3. Sometimes, as in pulse 400, the two signals are coincident, sometimes, as in pulse 402, the jittered signal is early, and sometimes, as in pulse 404, the jittered signal is late. Introducing a

small random noise into the pulse modulated signal spreads the spectral properties of the pulse frequency (which is the ripple frequency of the analog output signal produced by low pass filtering of the pulse modulated signal).

It will be appreciated by persons skilled in the art that the present invention is not limited by what has been particularly shown and described herein above. Rather the scope of the invention is defined by the claims that follow:

CLAIMS

What is claimed is:

1. A switchable low pass filter comprising:

a first switch connected to a first resistive element;

a second switch connected to a second resistive element;

a capacitive element connected to said first resistive element and said second resistive element; and

a controller connected to said first switch and said second switch, said controller operative to open and close at least one of said first switch and said second switch.

2. A switchable low pass filter according to claim 1, wherein said first resistive element has a resistance which is smaller than the resistance of said second resistive element.

3. A device comprising:

a plurality of resistive elements;

at least one switch connected to one of said resistive elements;

a capacitive element connected to said resistive elements thereby forming a low pass filter with said resistive elements; and

a controller connected to said at least one switch, said controller operative to open and close said at least one switch thereby switching the resistance of said low pass filter.

4. A device comprising:

a plurality of resistive elements;

at least one switch connected to one of said resistive elements;

a capacitive element connected to said resistive elements thereby forming a low pass filter with said resistive elements, said low pass filter having a response time; and

a controller connected to said at least one switch, said controller operative to open and close said at least one switch thereby changing said response time.

5. A digital to analog converter comprising:

a digital circuit which produces a pulse modulated signal; and

a switchable low pass filter having a plurality of response times for converting said pulse modulated signal to an analog signal having ripples,

wherein switching said low pass filter among said response times changes the size of said ripples.

6. A digital to analog converter according to claim 5, wherein said digital circuit is a pulse width modulation circuit.

7. A digital to analog converter according to claim 5, wherein said digital circuit is a pulse density modulation circuit.

8. A digital to analog converter according to claim 5, wherein said switchable low filter comprises:

a first switch connected to a first resistive element;

a second switch connected to a second resistive element;

a capacitive element connected to said first resistive element and said second resistive element; and

a controller connected to said first switch and said second switch, said controller operative to open and close at least one of said first switch and said second switch.

9. A digital to analog converter according to claim 8, wherein said first resistive element has a resistance which is smaller than the resistance of said second resistive element.

10. A device for producing a pulse density modulated signal whose pulse timing is jittered, the device comprising:

a flip flop for storing a value;

a random number generator for producing a substantially random number; and

an adder for adding said substantially random number and a multi-bit number to said value, said adder having an upper limit,

wherein a pulse is produced when the sum of said substantially random number, said multi-bit number and said value is not less than said upper limit.

11. A method for producing a pulse density modulated signal whose pulse timing is jittered, the method comprising the steps of:

adding a substantially random number and a multi-bit number to a value stored in a flip flop, thereby producing a sum;

if said sum is less than an upper limit, storing said sum in said flip flop, thereby replacing said value;

if said sum is not less than said upper limit,

producing a pulse;

subtracting said upper limit from said sum, thereby producing a result; and

storing said result in a flip flop; and

repeating said steps.

ABSTRACT

A switchable low pass filter includes a first switch connected to a first resistive element, a second switch connected to a second resistive element, and a capacitive element connected to the first and second resistive elements. The switchable low pass filter also includes a controller connected to the first switch and the second switch, the controller operative to open and close at least one of the first switch and the second switch. A method for producing a pulse density modulated signal whose pulse timing is jittered includes the following steps: adding a substantially random number and a multi-bit number to a value stored in a flip flop, thereby producing a sum; if the sum is less than an upper limit, storing the sum in the flip flop, thereby replacing the value; if the sum is not less than the upper limit, producing a pulse, subtracting the upper limit from the sum, thereby producing a result, and storing the result in a flip flop; and repeating the steps.

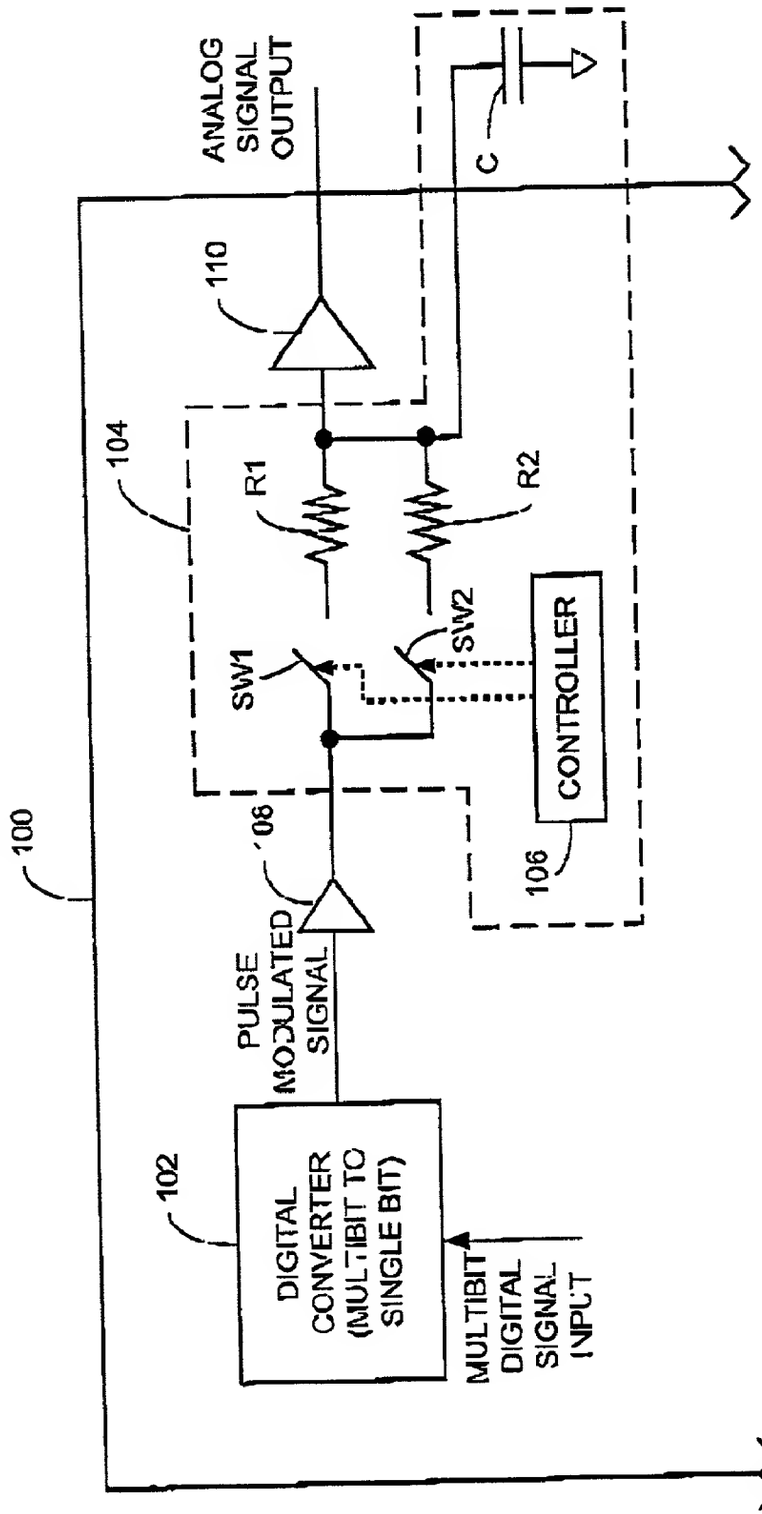
ANALOG SIGNAL OUTPUT
C
110
104
R1
R2
SW1
SW2
CONTROLLER
106
108
100
PULSE MODULATED SIGNAL
102
DIGITAL CONVERTER (MULTIBIT TO SINGLE BIT)
MULTIBIT DIGITAL SIGNAL INPUT

FIG. 1

FIG. 2A

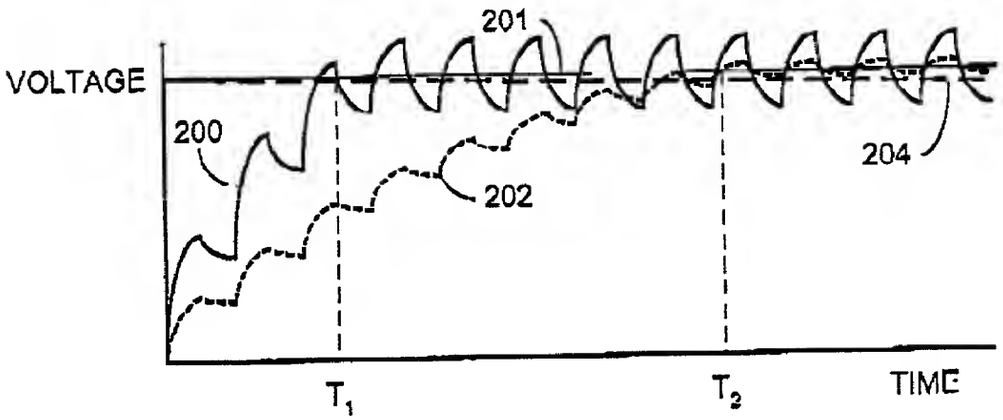

FIG. 2B

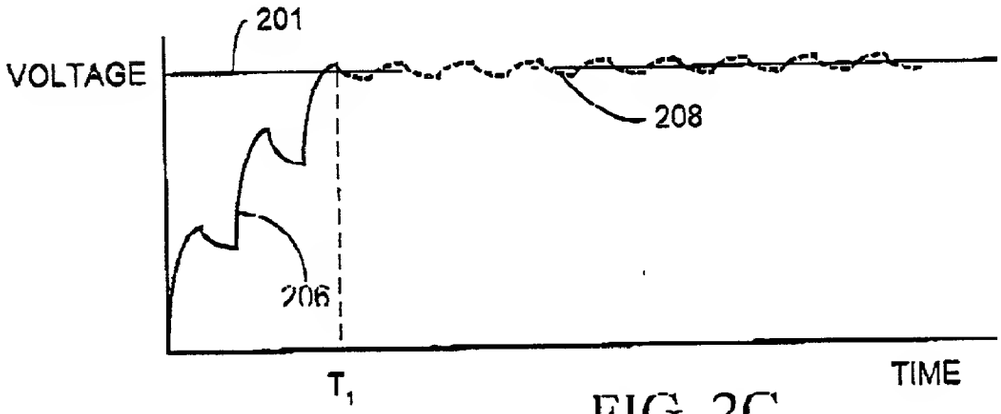

FIG. 2C

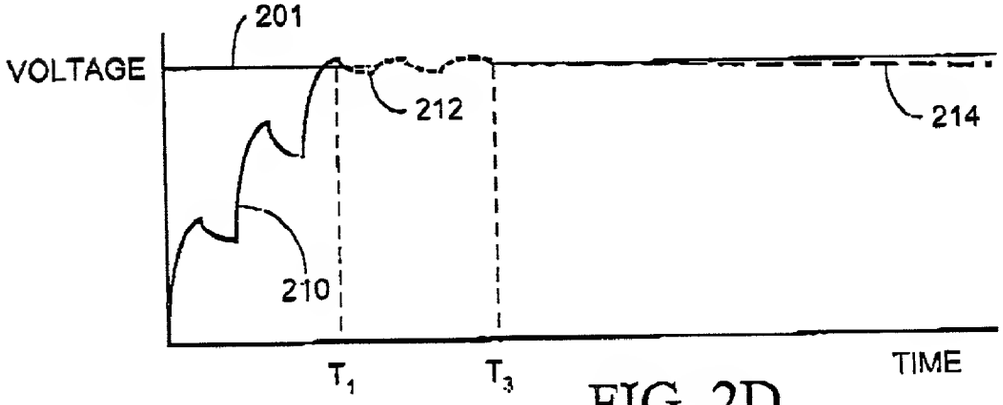

FIG. 2D

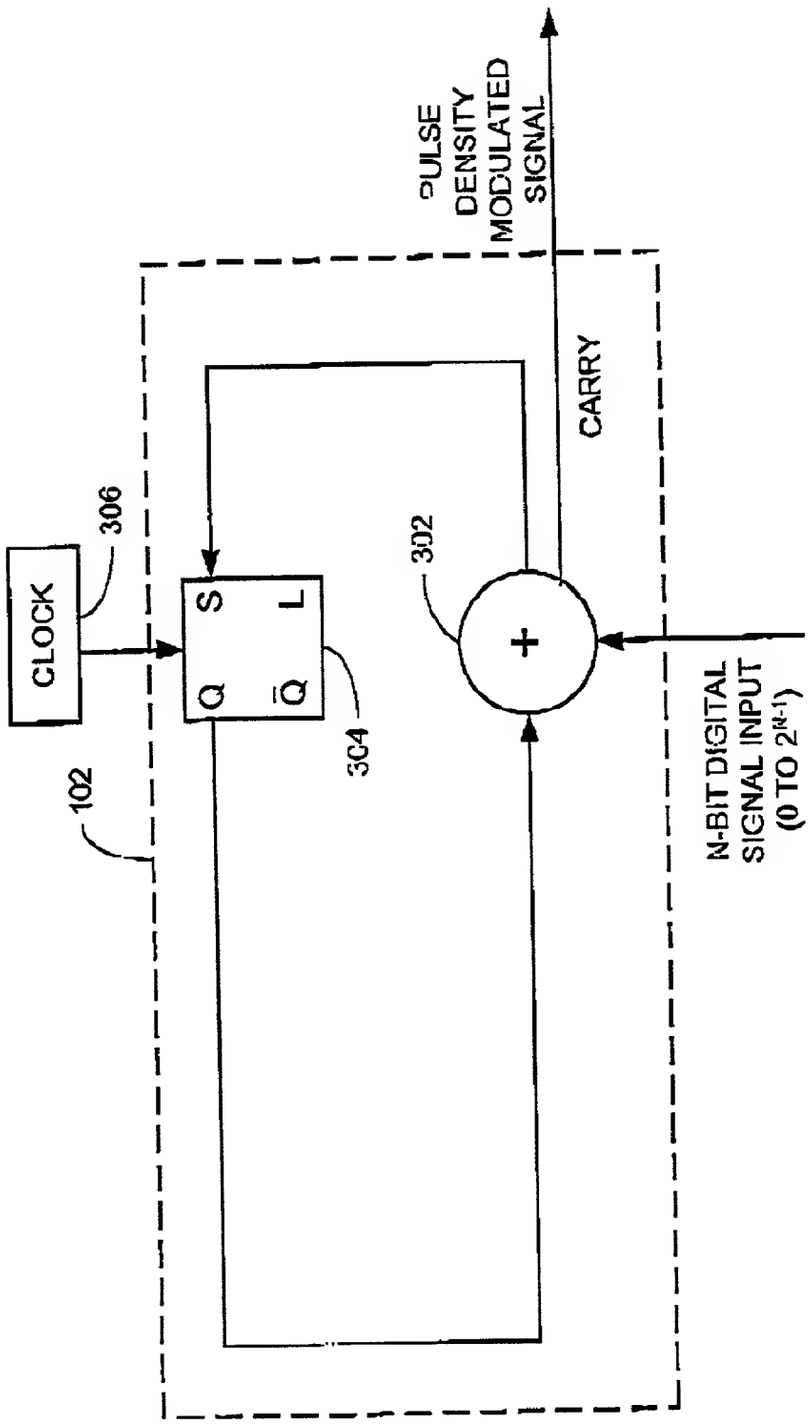
PULSE DENSITY MODULATED SIGNAL
CARRY
CLOCK
306
S
L
Q
$\bar{Q}$
304
302
102
N-BIT DIGITAL SIGNAL INPUT (0 TO 2^{N-1})
+

FIG. 3

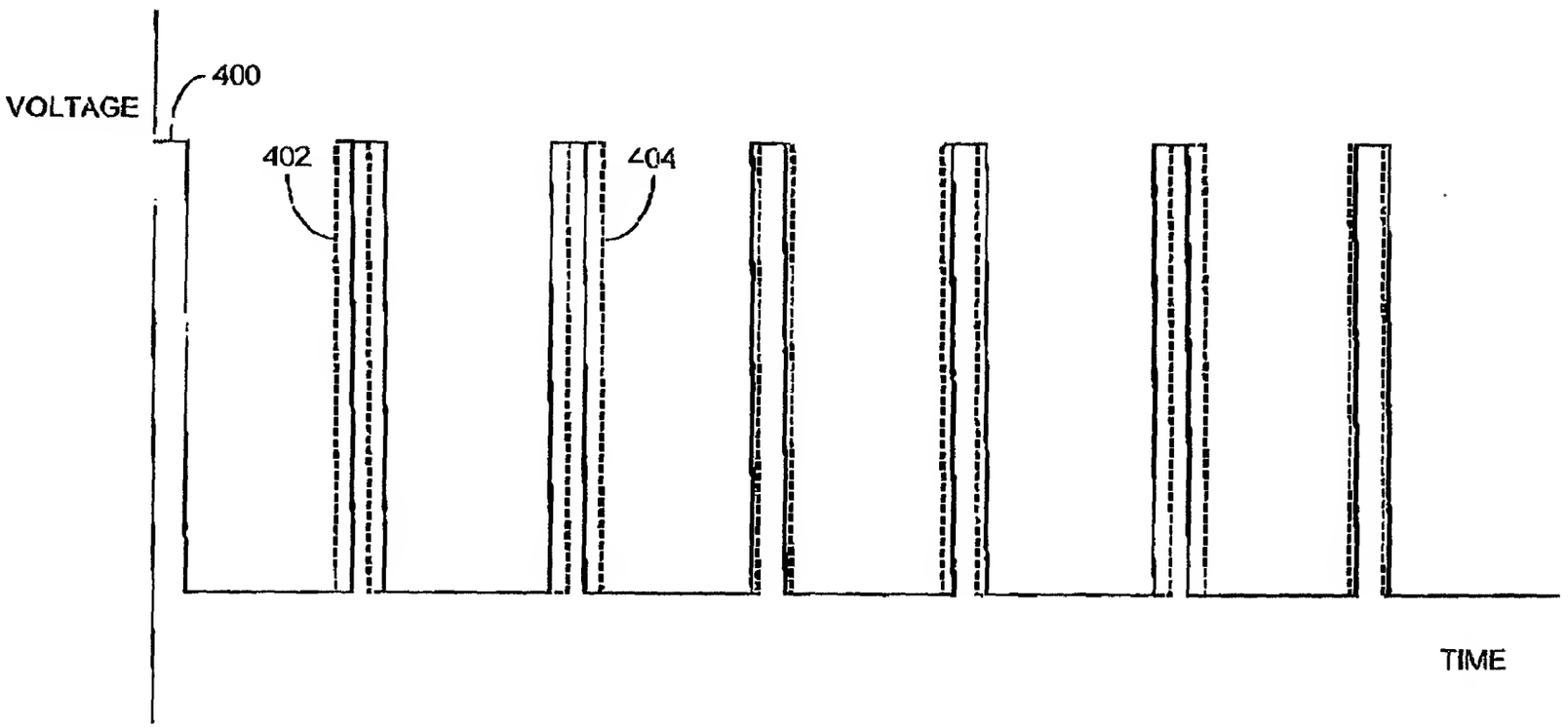

FIG. 4

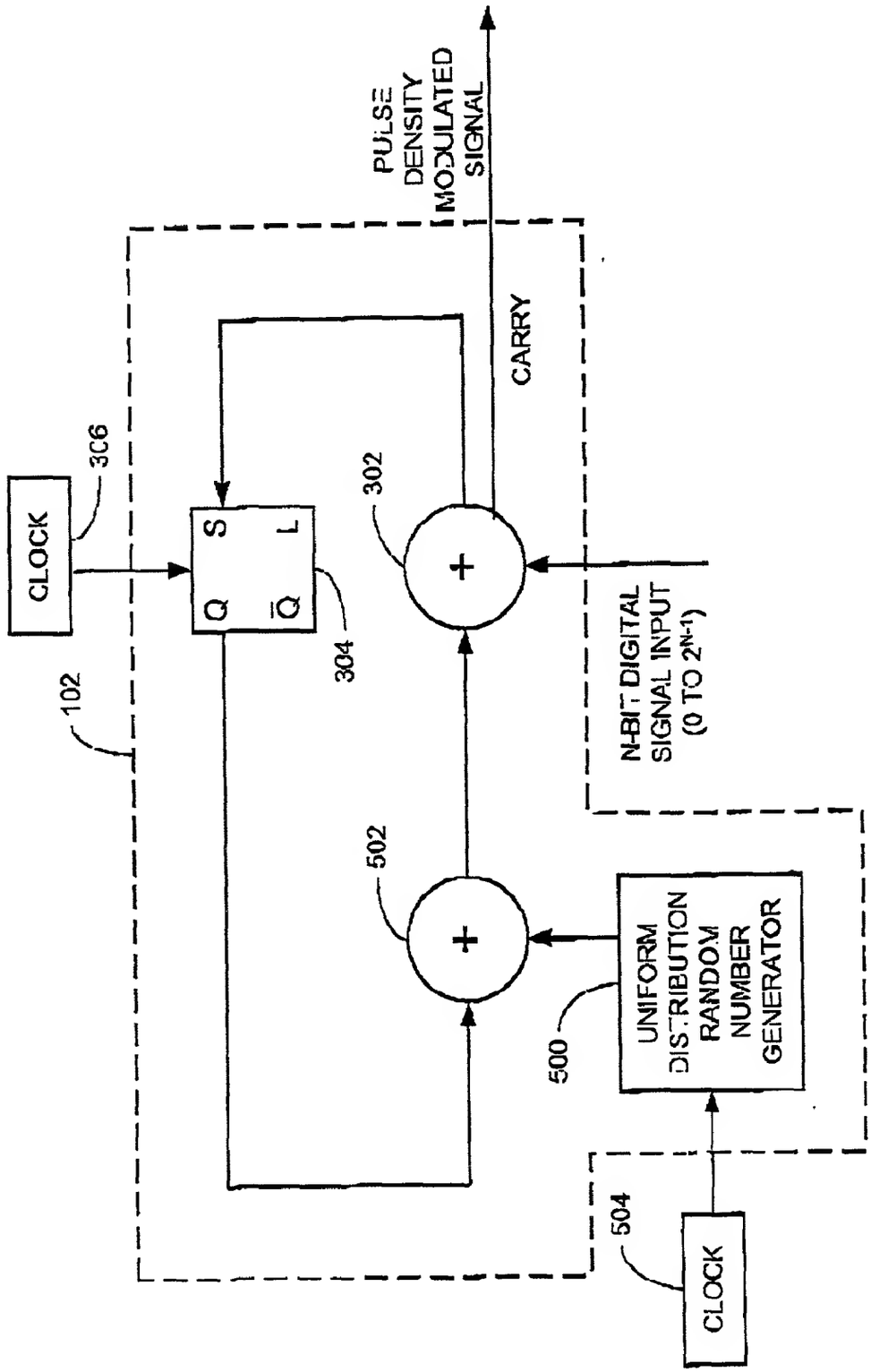
PULSE DENSITY MODULATED SIGNAL
CARRY
CLOCK
306
S
L
Q
$\bar{Q}$
304
302
+
N-BIT DIGITAL SIGNAL INPUT (0 TO 2^{N-1})
102
502
+
UNIFORM DISTRIBUTION RANDOM NUMBER GENERATOR
500
504
CLOCK

FIG. 5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
DECLARATION FOR PATENT APPLICATION

INVENTOR(S): **Eran GURFINKEL, Daniel YELLIN, Shlomo YAKOBOVICH and Arie STALBERG**

TITLE : **PULSE MODULATED DIGITAL TO ANALOG CONVERTER (DAC)**

DOCKET NO. : **P-2588-US**

TO THE HONORABLE COMMISSIONER OF PATENTS AND TRADEMARKS:

As a below named inventor, I hereby declare that:

This declaration is of the following type: (check one applicable item below)

- ☒ original
- ☐ design
- ☐ supplemental

NOTE: *If the declaration is for an International Application being filed as a divisional, continuation or continuation-in part application do not check next item; check appropriate one of last three items.*

- ☐ national stage of PCT

And is a

- ☐ divisional
- ☐ continuation
- ☐ continuation-in-part (CIP)

of U.S. Patent Application

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **PULSE MODULATED DIGITAL TO ANALOG CONVERTER (DAC)**, the specification of which is attached hereto unless the following is checked:

☐ was filed on as United States Application Number or PCT International Application Number , and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 (see last page attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a) - (d) or 265(b) of any foreign application(s) for patent or inventor's certificate or 365(a) of any PCT international application which designates at least one country other than the United States of America, listed below and have also identified below any foreign application for patents or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications:			Priority Claimed:	
(Number)	(Country)	(Day/Month,Year Filed)	☐ Yes	☐ No

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

(Application No.)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the National or PCT international filing date of this application.

(Application No.)	(Filing Date)	(Status - patented, pending, abandoned)
(Application No.)	(Filing Date)	(Status - patented, pending, abandoned)

As the inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the U.S. Patent and Trademark Office connected therewith. Name and registration number are listed below.

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MARK S. COHEN	42,425
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JOHN L. WELSH	33,621
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Date: _____ Signature: _____

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§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim is issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventory may comply with this section by disclosing information to the attorney, agent, or inventor.